REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This amendment is in response to the Office Action dated September 16, 2003. By the present amendment, the original claims 1-13 have been cancelled, without prejudice. In place of the original claims, new claims 14-25 have been added. These new claims have been drafted to specifically address and overcome the issues set forth in the 35 U.S.C. § 112, second paragraph, rejection with regard to the original claims 3, 4, 5/3, 8, 9, 10, 12 and 13 beginning on page 6 of the Office Action. Accordingly, removal of this rejection is respectfully requested. It is noted that there is presently no claim corresponding to the original claim 11. As such, the 35 U.S.C. § 112, first and second paragraph rejections, as well as the objections to the drawings concerning claim 11, are obviated by this response (noting, however, that the Applicant reserves the right to submit additional claims corresponding to claim 11 in the future).

Also by the present amendment, Figs. 9 and 10 of the drawing have been amended to the response to the objections to the claims set forth in the first two paragraphs on page 2 of the Office Action. Accordingly, removal of the objections set forth in these first two paragraphs on page 2 of the Office Action is respectfully requested.

Briefly, the present invention is directed to an improved arrangement of a semiconductor device and a multilayer wiring board. Referring to Fig. 1, solely for purposes of example, one embodiment of the present invention is shown illustrating an arrangement of a semiconductor device 1 and a multilayer wiring board 3. As

discussed on page 16 of the specification, the semiconductor device 1 is aligned with the multilayer wiring board 3 in such a manner that a through hole or via 5 in the semiconductor device 1 is aligned to at least partially overlap an area where a through hole or via 4 is provided in the multilayer wiring board 3. By virtue of this, the via 5, which is plated with a conductive material, and the thermal via 4, which is filled with a thermally and electrically conductive material, are at least partially aligned with one another so that they are both thermally and electrically connected. As discussed on page 19, this significantly improves the discharge of heat in a thickness-wise direction that is generated from the semiconductor device.

Reconsideration and removal of the 35 U.S.C. § 102 and 103 rejections set forth in the Office Action based on either Shirakawa (1077494) and/or the admitted prior art is respectfully requested. Newly submitted claims 14-25 clearly define features of the present invention which are not at all suggested by either Shirakawa or the admitted prior art. With regard to Shirakawa, it is noted that this reference fails to describe any detailed arrangement of a wiring board side to read on the feature set forth in the present claims. Similarly, nothing in the admitted prior art teaches the claimed arrangements. For example, in claims 14 and 15 and their dependent claims, a particular alignment of the through holes of the semiconductor substrate and the through holes of a multilayer wiring board is set forth such that the through holes in the semiconductor substrate are either entirely or at least partially overlapped by through holes of the multilayer wiring board. New independent claim 17 defines the location of the heat dissipating regions in the semiconductor substrate being located inside of a through hole or an area where the through holes are built into a multilayer wiring board. New claim 17 defines the arrangement of the through

holes of the semiconductor substrate and the multilayer wiring board in combination with the one dimensional heat flow through these through holes. New independent claim 22 defines the in-plane distribution of heat from transistors of the semiconductor substrate coinciding substantially with the distribution of cross-plane through holes in the multilayer wiring board. Claim 23 defines a wiring board with a claimed relationship between the through holes of the semiconductor substrate and the through holes in the multiwiring board. Claim 24 specifically defines a semiconductor device including a plurality of finger shaped emitter electrodes or source electrodes with at least one via hole arranged in rows in a first direction on the semiconductor substrate with specific recitations concerning the rows. It is respectfully submitted that none of these features are found either in Shirakawa or the admitted prior art. Therefore, reconsideration and allowance of the newly submitted claims 14-25 over the cited prior art is respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus,

LLP Deposit Account No. 01-2135 (Docket No. 500.40530X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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FIG.9

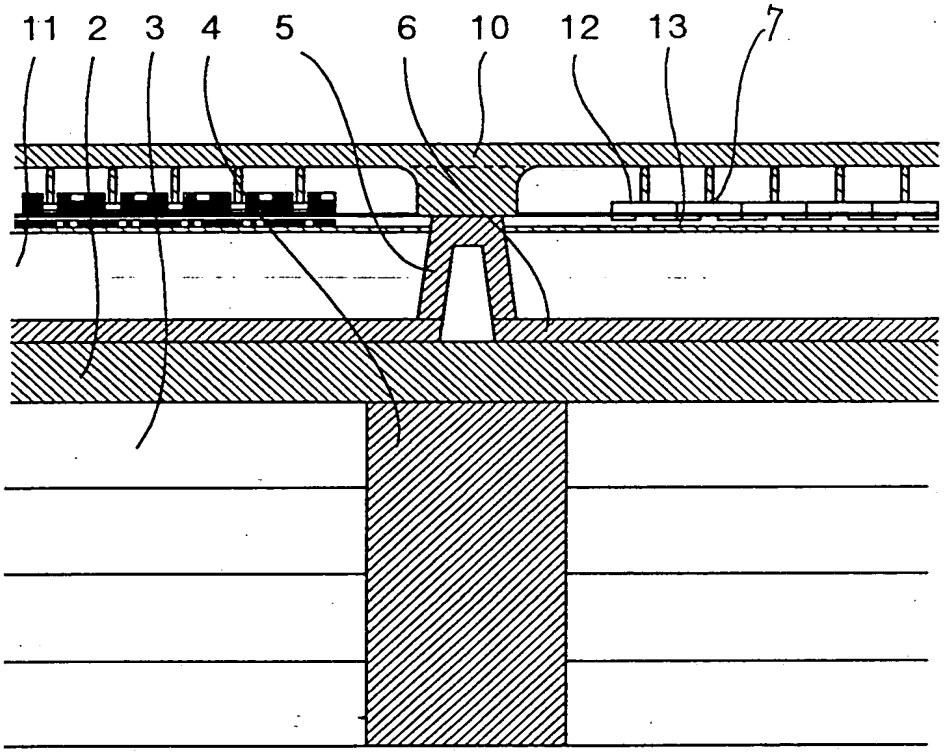

FIG.10